Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.035”**

**G**

**SOURCE**

**.055”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .004 x .004”**

**Backside Potential: DRAIN**

**Mask Ref: B4658**

**APPROVED BY: DK DIE SIZE .035” X .055” DATE: 8/31/21**

**MFG: VISHAY THICKNESS .010” P/N: SI3433**

**DG 10.1.2**

#### Rev B, 7/1